Development of an Organic Wafer-level Packaging Platform for Highly Integrated RF Transceivers

R. Ramachandran and A. Pham

Clemson Integrated Microsystems Group (CIM)
Holcombe Department of Electrical and Computer Engineering
Clemson University, Clemson, SC 29634

Abstract - **We present the development of a novel organic-micromachined packaging scheme at the wafer level for highly integrated RF transceivers. This process enables the integration of on-chip passive devices and isolation structures at the wafer level. We demonstrate the development of inductors that achieve a Q-factor of about 61 at 1.7 GHz and on-chip isolation structures that provide an isolation of more than 50 dB in the GHz range.**

I. INTRODUCTION

With the ever-increasing growth in personal wireless communications, manufacturers are driven for the design of smaller and lighter hand-held devices with increasing functionality. These demands require new packaging schemes that enable the implementation of highly integrated transceivers. An approach to realize highly integrated RF transceiver systems is to migrate off-chip components onto Si integrated circuits (ICs) that contain the workhorse of digital processing power. However, integrated passive devices including transmission lines, filters, and inductors suffer significant losses due to low resistivity Si substrates at RF frequencies. Furthermore, highly integrated transceivers must have high isolation to house a receiver, a transmitter, and mixed-signal circuitry on the same wafer chip. Although microelectromechanical (MEM) passive elements on Si are attractive for high-frequency applications, the insertion of RF MEMs will only take place for structures that are fully compatible with monolithic integration. For this reason, RF MEMs has not been widely inserted onto mainstream ICs [1,2]. Other techniques include the deposition of a polymer layer onto a host substrate for design of multi-layer structures. These techniques have been used in multi-chip module (MCM-D) applications [3,4]. Demonstrations of polymer-deposited structures have been limited to thin film layers that are not attractive for designing low-conductor loss interconnects and passive devices.

In this paper, we present the development of an organic-micromachined process that enables the packaging and integration of highly integrated transceivers. This process allows for a fabrication of an ultra-thick polymer layer that can be processed using standard lithography techniques to create micromachined structures and interconnects. Hence, the organic packaging process not only provides the integration of high-performance micromachined on-chip passive devices and interconnects but also enables the realization of novel isolation structures for highly integrated systems. Using this process, we have already demonstrated low-loss micromachined transmission lines on Si, which achieve a measured attenuation of 0.18 dB/cm at 20 GHz [5]. At this conference, we will demonstrate the development of a novel on-chip inductor that achieves a Q-factor of 61 at 1.7 GHz and an improved process to increase the SU-8 thickness. We also propose a novel isolation scheme that can provide RF signal separation of at least 50 dB in the GHz regime

II. ORGANIC BASED PACKAGING PROCESS

The SU-8 based UV-LIGA (a German acronym for electroplating, lithography, and molding) process developed at Clemson University is the enabling fabrication technique for wafer level packaging. This process employs a negative photoresist SU-8 that can be spin-coated to achieve ultra-thick films that have excellent sensitivity, high resolution, low optical absorption, and thermal stability [6]. Some of the basic processing steps of SU-8 can be found in [5-8]. The process begins by coating a wafer with a solution containing Dupont VM 651 to adhere SU-8 to Si (7.2 Ω-cm). The ultra-thick photoresist is then spun onto the wafer to achieve a desired thickness. This wafer is then soft baked on the hotplate for 1.5 hours at a temperature of 95 °C. To create patterns, the SU-8 is exposed to UV light (350-450 nm wavelength) using a dark field mask for about 540 seconds. After the exposure, the wafer is baked for 1 hour at 95 °C to fully imidize the photoresist that becomes highly resistant to a developer solution. The

0-7803-7239-5/02/$10.00 © 2002 IEEE

ultra-thick photoresist is developed in a propylene glycol methyl ether acetate solution (PGMEA) to form micromachined structures. A thin layer of chrome and gold are then deposited on the micromachined structures. The thickness of the gold on the micromachined structures is then increased to about 4-5μm by electroplating techniques to form circuitry. In this packaging platform, the polymer layer will remain on top of a Si substrate. The polymer structure can be micromachined to develop high performance RF circuitry including on-chip inductors, low-loss transmission lines, filters, and isolation walls. Several types of SU-8 are available with a variety of coefficients of thermal expansion to reduce stress between the thick polymer layer and Si. Figure 1 demonstrates the schematic representation of the organic-micromachined packaging platform.

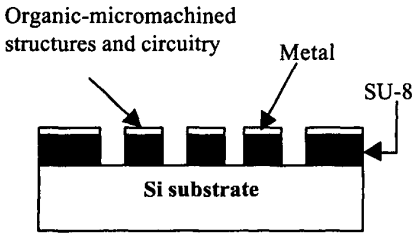

Figure 1. A cross section representation of the organic-micromachined packaging platform on Si

III. ON-CHIP ORGANIC-MICROMACHINED INDUCTORS

The fabricated on-chip inductor is a 1-turn, one port, rectangular spiral inductor. The spiral conductor is supported by SU-8 that can be processed and partially removed to leave air as a main substrate. The thickness of the supporting SU-8 is 200μm in this work and can be varied to achieve optimal performance. Hence, the electromagnetic fields are influenced by the combination of SU-8 and air that has no tangent loss. Figure 2 shows the SEM picture of an on-chip inductor fabricated at Clemson University.

We utilize a Cascade probe station, a Network Analyzer HP8510C, and CPW probes for electrical characterization. Prior to measurements a one-port on-wafer calibration is performed to establish reference planes at the probe tips. Based on the S-parameter measurements, an equivalent circuit model is developed and optimized to extract the parasitic elements. The model consists of an ideal inductor L_s in series with a resistance R_s to account for conductor loss, a parallel resistance R_p to account for SU-8 dielectric loss, and a capacitance C_p representing both the substrate capacitance and the dielectric capacitance (Figure 3). The measured Q-factor for the inductor is calculated by taking the ratio of the imaginary part to the real part of the input impedance and the measured effective inductance is obtained from the imaginary part of the input impedance. The on-chip micromachined inductor achieves a Q-factor of 61 at 1.7 GHz. Figure 4 demonstrates that the effective inductance value increases with a drop in the Q-factor. Further improvements in the Q-factor are expected with increase in the dielectric height and plasma etching techniques to remove SU-8 from underneath the conductor.

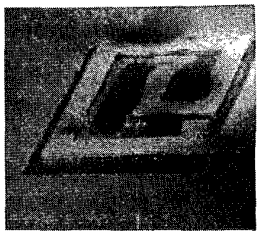

Figure 2. A SEM picture of the micromachined inductor

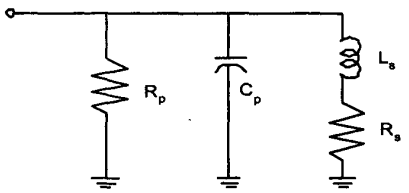

Figure 3. The Equivalent circuit model for micromachined inductor. L_s = 1.9 nH, R_p = 1.5 KΩ, C_p = 570.6 fF, R_s = 0.7 Ω

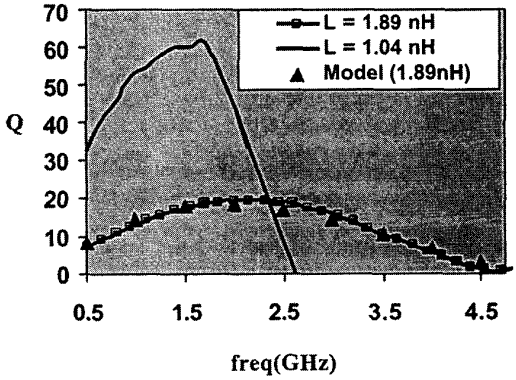

Figure 4. Measured Q-factors of the micromachined inductors with different inductance values

IV. ISOLATION STRUCTURES

We expect that the future development of our process will evolve the integration of highly integrated transceivers. On the same chip, integrated passive devices, RF receivers and transmitters will be housed with digital circuitry as shown in figure 5. We have developed the concept of micromachined metal wall structures with backside etching of the substrate to provide on-chip isolation mechanisms. The isolation can be achieved by tall SU-8 structures micromachined directly above a groove on the back side of the substrate. The SU-8 wall acts as a barrier between the two devices under consideration. The metal walls act as an effective RF ground for the devices thereby reducing noise and cross-talk. Also the back-side etch of the substrate minimizes the signal coupling across the devices through the substrate. The walls are metallized with electroplated gold. Another substrate with gold metallization is then assembled onto the SU-8 walls as shown in figure 7. Figure 6 demonstrates the fabrication of 700μm tall micromachined structures that can be used as metal bars for electromagnetic shielding. At the conference, we will present the process of achieving anisotropic etch of the back-side of the silicon wafer for implementing the isolation scheme. Using this platform, we have conducted electromagnetic analysis using Ansoft's High Frequency Structure Simulator to investigate the feasibility of these structures. In the simulation, a 700μm tall SU-8 wall was introduced between two microstrip lines, with a backside etch of the silicon wafer directly underneath the SU-8 wall. A metal layer was then placed on top of the SU-8 wall so as to provide complete electromagnetic shielding. The electromagnetic simulations demonstrate that 55-dB isolation can be achieved using this novel on-chip isolation scheme (Figure 8).

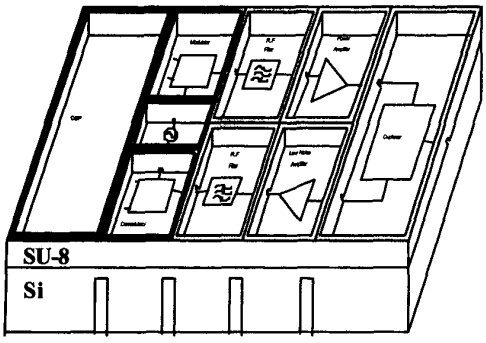

Figure 5. A highly integrated transceiver

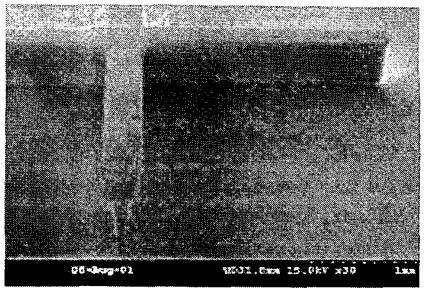

Figure 6. A prototype of a 700μm-tall micromachined structure that can be used for on-chip isolation

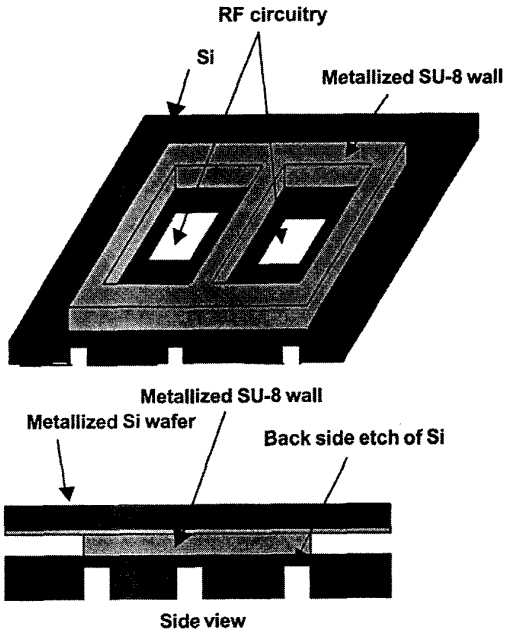

Figure 7. Illustration of isolation scheme using SU-8 micromachining

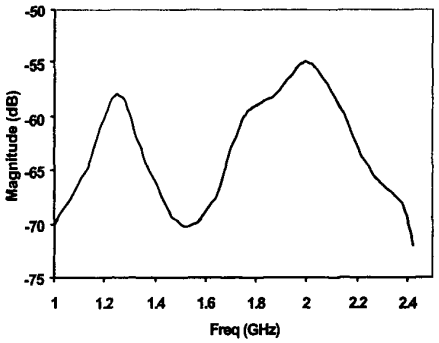

Figure 8. Simulated results of isolation

V. CONCLUSION

We present the development of an organic-micromachined packaging scheme at the wafer level for highly integrated RF transceivers. This process enables the integration of on-chip passive devices and isolation structures at the wafer level. We demonstrate the development of on-chip inductors that achieve a Q-factor of about 61 at 1.7 GHz. With the ability to micromachine high aspect ratio SU-8 structures, the potential of this technology for RF applications is limitless. The on-chip isolation structures provide an isolation of at least 55 dB in the GHz range and can serve as efficient isolation mechanisms to house a receiver, transmitter and mixed signal circuitry on the same chip.

ACKNOWLEDGEMENT

The authors would like to acknowledge the support in part by the National Science Foundation Packaging Research Center at the Georgia Institute of Technology under contract EE-092723 and the NSF CAREER award for Prof. Pham under award ECS-0093525.

REFERENCES

[1] S. V. Robertson, A. R. Brown, L. P. B Katehi, and G. M. Rebeiz, "A 10-60-GHz micromachined directional coupler," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, pp. 1845-1849, Nov. 1998.

[2] K. J. Herrick, T. A. Schwarz, and L. P. B. Katehi, "Si-micromachined coplanar waveguides for use in high-frequency circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, pp. 762-768, June 1998.

[3] K. Kamogawa, T. Tokumitsu, and M. Aikawa, "Multifrequency microstrip antennas using alumina-ceramic/polyimide multiplayer dielectric substrate," *IEEE Trans. on Microwave Theory and Techniques*, vol. 44, pp. 2413-2437, Dec. 1996.

[4] M. Nakatsugawa, A. Kanda, H. Okazaki, K. Nishikawa, and M. Muraguchi, "Line-loss and size reduction techniques for millimeter-wave RF front-end boards by using a polyimide/alumina-ceramic multiplayer configuration," *IEEE Trans. on Microwave Theory and Techniques*, vol. 45, pp. 2308-2325, Dec. 1997.

[5] D. Newlin, A. Pham, J. Harriss, and J. B. Lee, "Development of an organic micromachining process on Silicon for RF/Microwave applications," in *34th International Symposium on Microelectronics Digest,* pp. 44-47, October 2001.

[6] J. .M. Shaw, J. D. Gelorme, N. C. LaBianca, W.E. Conley and S. J. Holmes, "Negative photoresists for opticallithography,"http://www.research.ibm.com/journal/rd/411/shaw.html.

[7] Automated SU-8 Resist Processing, Electronic Visions Application Notes, 3701 E. University Drive, Suite 300.

[8] R. Ramachandran, D. Newlin and A. Pham, "Development of RF/Microwave on-chip inductors using an Organic micromachining process," *IEEE EPEPDigest*, pp. 97-100, Oct. 2001.